What is claimed is:

1. A single-crystal silicon substrate, comprising:

an oxidized film, a gate pattern, and an impurity ion implanted interface on a surface of the single-crystal silicon substrate, and the surface is planarized after forming the oxidized film, the gate pattern, and the impurity ion implanted interface, and

a dense position of implanted hydrogen ions, to which a predetermined concentration of hydrogen ions is implanted for a predetermined depth.

2. A single-crystal silicon substrate, comprising:

an impurity ion implanted/diffused area in which a PNP junction structure or an NPN junction structure, to which impurity ions are implanted, is provided near a surface of the single-crystal silicon substrate; and

an oxidized film formed on the impurity ion implanted/diffused area.

3. The single-crystal silicon substrate as defined in claim 2, further comprising a dense position of implanted hydrogen ions, to which a predetermined concentration of hydrogen ions is implanted for a predetermined depth.

4. The single-crystal silicon substrate as defined in claim 1, wherein, a thickness of the oxidized film is not less than 200nm.

5. The single-crystal silicon substrate as defined in claim 2, wherein, a thickness of the oxidized film is not less than 200nm.

6. An SOI substrate in which a single-crystal thin film is provided on an insulating substrate, comprising:

a bonded interface at which an insulating film formed on the insulating substrate is bonded with a covering film with which the single-crystal silicon substrate is covered,

the single-crystal silicon substrate being separated at a dense position of implanted hydrogen ions so that the single-crystal silicon thin film is formed,

the insulating substrate being a light-transmitting substrate, and

the single-crystal silicon substrate being separated by means of heat treatment.

7. An SOI substrate in which a single-crystal silicon thin film is provided on an insulating substrate, comprising:

a bonded interface at which an insulating film formed on the insulating substrate is bonded with a covering film with which a single-crystal silicon substrate is covered,

the single-crystal silicon thin film being formed by separating the single-crystal silicon substrate at a dense position of implanted hydrogen ions by means of heat treatment, and

at the bonded interface, the insulating film is arranged to satisfy that a $\tan\theta$ is not more than 0.06, where θ is the angle between (i) a maximum slope curve of micro-roughness, the micro-roughness being measured in a 1-5μm square and not more than 5nm in height, and (ii) an average surface plane.

8. An SOI substrate in which a single-crystal silicon thin film is provided on an insulating substrate, comprising:

a bonded interface at which an insulating film formed on the insulating substrate is bonded with a covering film with which a single-crystal silicon substrate is covered,

the single-crystal silicon thin film being formed by separating the single-crystal silicon substrate at a dense position of implanted hydrogen ions by means of heat

treatment, and

contact angles of a surface of the insulating film and a surface of the covering film with respect to water being not more than 10°.

9. An SOI substrate in which a single-crystal silicon thin film is provided on an insulating substrate, comprising:

a bonded interface at which an insulating film formed on the insulating substrate is bonded with a covering film with which a single-crystal silicon substrate is covered,

the single-crystal silicon thin film being formed by separating the single-crystal silicon substrate at a dense position of implanted hydrogen ions by means of heat treatment, and

the insulating film being an oxidized silicon film formed by a plasma chemical vapor deposition method using a gas mixture of a TEOS gas and an oxygen gas.

10. An SOI substrate in which a single-crystal silicon thin film is provided on an insulating substrate, comprising:

a bonded interface at which an insulating film formed on the insulating substrate is bonded with a

covering film with which a single-crystal silicon substrate is covered,

the single-crystal silicon thin film being formed by separating the single-crystal silicon substrate at a dense position of implanted hydrogen ions by means of heat treatment, and

at the bonded interface, the insulating film which is made of oxidized silicon and 5-300nm thick being bonded.

11. An SOI substrate in which a single-crystal silicon thin film is provided on an insulating substrate, comprising:

a bonded interface at which an insulating film formed on the insulating substrate is bonded with a covering film with which a single-crystal silicon substrate is covered,

the single-crystal silicon thin film being formed by separating the single-crystal silicon substrate at a dense position of implanted hydrogen ions by means of heat treatment, and

a adhesive strength at the bonded interface being not less than 0.6N/m.

12. The SOI substrate as defined in claim 6, wherein, a single-crystal thin-film device is formed on the

single-crystal silicon substrate, and the single-crystal thin-film contains the single-crystal thin-film device being formed by separating the single-crystal silicon substrate at the dense position by means of heat treatment.

13. The SOI substrate as defined in claim 7, wherein, a single-crystal thin-film device is formed on the single-crystal silicon substrate, and the single-crystal thin-film contains the single-crystal thin-film device being formed by separating the single-crystal silicon substrate at the dense position by means of heat treatment.

14. The SOI substrate as defined in claim 6, further comprising:

a single-crystal silicon thin-film device manufactured from the single-crystal silicon thin film; and

a non-single-crystal silicon thin-film device which is manufactured from a non-single-crystal silicon thin film provided in an area on the insulating substrate, the area being different from an area where the single-crystal silicon thin film is provided.

15. The SOI substrate as defined in claim 7, further comprising:

a single-crystal silicon thin-film device manufactured

from the single-crystal silicon thin film; and

a non-single-crystal silicon thin-film device which is manufactured from a non-single-crystal silicon thin film provided in an area on the insulating substrate, the area being different from an area where the single-crystal silicon thin film is provided.

16. A semiconductor device, comprising: a non-single-crystal silicon thin-film device manufactured from a non-single-crystal silicon thin film and a single-crystal silicon thin-film device manufactured from a single-crystal silicon thin film,

wherein the non-single-crystal silicon thin-film device and the single-crystal silicon thin-film device are provided in different areas of an insulating substrate.

17. The semiconductor device as defined in claim 16, wherein, the single-crystal silicon thin-film device is bonded with the insulating substrate via an intervening inorganic insulating film.

18. The semiconductor device as defined in claim 16, wherein, each of the non-single-crystal silicon thin-film device and the single-crystal silicon thin-film device is either a MOS thin-film transistor or a MIS thin-film

transistor.

19. The semiconductor device as defined in claim 18, wherein, in the MOS thin-film transistor, a gate, a gate insulating film, and a silicon are formed on the insulating substrate in this order.

20. The semiconductor device as defined in claim 18, wherein, a thickness of a silicon thin film of the MOS thin-film transistor is about not more than 600nm.

21. The semiconductor device as defined in claim 18, wherein, a thickness of a single-crystal silicon thin film of the MOS thin-film transistor is about not more than 100nm.

22. The semiconductor device as defined in claim 18, wherein, a metal pattern of the MOS single-crystal silicon thin-film transistor is formed under a wiring rule which is more relaxed than a wiring rule of a gate pattern of the MOS single-crystal silicon thin-film transistor.

23. The semiconductor device as defined in claim 17, wherein, the non-single-crystal silicon thin-film device is either a MOS non-single-crystal silicon thin-film

transistor or a MIS non-single-crystal silicon thin-film transistor, and the single-crystal silicon thin-film device is a bipolar single-crystal silicon thin-film transistor.

24. The semiconductor device as defined in claim 17, wherein, the non-single-crystal silicon thin-film device is either a MOS non-single-crystal silicon thin-film transistor or a MIS non-single-crystal silicon thin-film transistor, and the single-crystal silicon thin-film device includes at least either one of a MOS single-crystal silicon thin-film transistor and a bipolar single-crystal silicon thin-film transistor.

25. The semiconductor device as defined in claim 17, wherein, the non-single-crystal silicon thin-film device is either a MOS non-single-crystal silicon thin-film transistor or a MIS non-single-crystal silicon thin-film transistor, and the single-crystal silicon thin-film device includes a MOS single-crystal silicon thin-film transistor, and an image sensor including a Schottky or PN-junction diode or a CCD image sensor.

26. The semiconductor device as defined in claim 24, wherein, a thickness of a single-crystal silicon thin-film of the MOS single-crystal silicon thin-film transistor is

thinner than a thickness of a single-crystal silicon thin film of the bipolar single-crystal silicon thin-film transistor.

27. The semiconductor device as defined in claim 23, wherein, the bipolar single-crystal silicon thin-film transistor has such a structure that a base area, a collector area, and an emitter area are formed and provided in one plane.

28. The semiconductor device as defined in claim 23, wherein, a metal wiring and a contact pattern of the bipolar single-crystal silicon thin-film transistor include respective parts each being formed in accordance with a wiring rule which is more relaxed than a wiring rule of a base pattern of the bipolar single-crystal silicon thin-film transistor.

29. The semiconductor device as defined in claim 23, wherein, a thickness of the single-crystal silicon thin film of the bipolar single-crystal silicon thin-film transistor is about not more than 800nm.

30. The semiconductor device as defined in claim 16, wherein, the non-single-crystal silicon thin film is either a

polycrystalline silicon thin film or a continuous grain silicon thin film, and a MOS thin-film transistor manufactured from the non-single-crystal silicon thin film includes a non-single-crystal silicon, a gate insulating film, and a gate on the insulating substrate in this order.

31. The semiconductor device as defined in claim 16, wherein, the non-single-crystal silicon thin film is either one of a polycrystalline silicon thin film or a continuous grain silicon thin film, and a MOS thin-film transistor manufactured from the non-single-crystal silicon thin film includes a gate, a gate insulating film, and a non-single-crystal silicon on the insulating substrate in this order.

32. The semiconductor device as defined in claim 16, wherein, the non-single-crystal silicon thin film is an amorphous silicon thin film, and a MOS thin-film transistor or a MIS thin-film transistor, which is manufactured from the non-single-crystal silicon thin film, includes a gate, a gate insulating film, and a non-single-crystal silicon on the insulating substrate in this order.

33. The semiconductor device as defined in claim 16,

wherein, the non-single-crystal silicon thin film is an amorphous silicon thin film, and a MOS thin-film transistor or a MIS thin-film transistor, which is manufactured from the non-single-crystal silicon thin film, includes a non-single-crystal silicon, a gate insulating film, and a gate on the insulating substrate in this order.

34. The semiconductor device as defined in claim 16, wherein, a difference of linear expansion between a single-crystal silicon constituting the single-crystal silicon thin-film device and the insulating substrate is about not more than 250ppm, within a temperature range from a substantially room temperature to 600°C.

35. The semiconductor device as defined in claim 16, wherein, the insulating substrate is a high strain point glass including an alkaline-earth alumino-borosilicate glass, and a SiO2 film is formed at least in an area on a surface of the insulating substrate, where the single-crystal silicon thin-film device is to be formed.

36. The semiconductor device as defined in claim 16, wherein, the insulating substrate is manufactured from at least one glass selected from the group consisting of a barium-borosilicate glass, a barium-alumino-borosilicate

glass, an alkaline-earth alumino-borosilicate glass, a borosilicate glass, an alkaline-earth zinc-lead-alumino-borosilicate glass, and an alkaline-earth zinc-alumino-borosilicate glass.

37. The semiconductor device as defined in claim 16, wherein, a margin of alignment of at least a part of a pattern on the single-crystal silicon is fine so as to be smaller than a margin of alignment of patterns on any one of an entire surface of a mother board, a display area, and an entirety of the non-single-crystal silicon thin-film device and the single-crystal silicon thin-film device.

38. The semiconductor device as defined in claim 16, wherein, an aligning mark formed on the single-crystal silicon is detected using visible light or light whose wavelength is shorter than the visible light, through a transparent substrate, and has a form which allows the aligning mark to be aligned with an aligning mark formed on the transparent substrate.

39. A display device, comprising:

an SOI substrate including a single-crystal silicon thin film provided on an insulating substrate, on the single-crystal silicon thin film a semiconductor device

structure being formed,

wherein, the SOI substrate includes a bonded interface at which an insulating film formed on the insulating substrate is bonded with a covering film with which a single-crystal silicon substrate is covered, the single-crystal silicon substrate is separated at a dense position of implanted hydrogen ions by heat treatment so that the single-crystal silicon thin film is formed, and the insulating substrate is a light-transmitting substrate.

40. A display device, comprising:

a semiconductor device in which a non-single-crystal silicon thin-film device and a single-crystal silicon thin-film device are provided on different areas of an insulating substrate,

the semiconductor device being used as an active matrix substrate of a display panel.

41. A method of manufacturing a semiconductor device in which a single-crystal silicon thin-film device manufactured from a single-crystal silicon thin film and a non-single-crystal silicon thin film are formed on an insulating substrate,

wherein, after a circuit including the single-crystal silicon thin-film device is formed on the insulating

substrate, the non-single-crystal silicon thin film is formed.

42. The method of manufacturing the semiconductor device as defined in claim 41, wherein, on the single-crystal silicon thin-film device, a protective interlayer insulating film, a contact hole, and a metal wiring are formed.

43. The method of manufacturing the semiconductor device as defined in claim 41, wherein, after the single-crystal silicon thin-film device is formed, an interlayer insulating film is formed, and then the non-single-crystal silicon thin film is formed.

44. A method of manufacturing a semiconductor device in which a single-crystal silicon thin-film device manufactured from a single-crystal silicon thin film and a non-single-crystal silicon thin film are formed on an insulating substrate,

wherein, after the non-single-crystal silicon thin film is formed on the insulating substrate, the single-crystal silicon thin-film device is formed.

45. The method of manufacturing the semiconductor

device as defined in claim 41, wherein, the single-crystal silicon thin-film device is a MOS single-crystal silicon thin-film transistor.

46. The method of manufacturing the semiconductor device as defined in claim 44, wherein, the single-crystal silicon thin-film device is a MOS single-crystal silicon thin-film transistor.

47. The method of manufacturing the semiconductor device as defined in claim 41, wherein, the single-crystal silicon thin-film device is a bipolar single-crystal silicon thin-film transistor.

48. The method of manufacturing the semiconductor device as defined in claim 44, wherein, the single-crystal silicon thin-film device is a bipolar single-crystal silicon thin-film transistor.

49. The method of manufacturing the semiconductor device as defined in claim 41, wherein, with respect to a single-crystal silicon substrate for manufacturing the single-crystal silicon thin-film device, a predetermined concentration of hydrogen ions is implanted for a predetermined depth.

50. The method of manufacturing the semiconductor device as defined in claim 44, wherein, with respect to a single-crystal silicon substrate for manufacturing the single-crystal silicon thin-film device, a predetermined concentration of hydrogen ions is implanted for a predetermined depth.

51. The method of manufacturing the semiconductor device as defined in claim 49, wherein, an energy for implanting the hydrogen ions is arranged so that an energy which is figured out by subtracting an energy corresponding to a projection range of the hydrogen ions, the projection range corresponding to a thickness of an oxidized film, from the energy for implanting the hydrogen ions is smaller than an energy corresponding to a projection range of atoms constituting a material in a layer formed on the oxidized film.

52. The method of manufacturing the semiconductor device as defined in claim 50, wherein, an energy for implanting the hydrogen ions is arranged so that an energy after subtracting an energy corresponding to a projection range of the hydrogen ions in a gate electrode material for a gate electrode thickness from an incident

energy of the hydrogen ions is no more than an energy corresponding to a projection range of the heaviest ions of gate constituent materials for a gate oxide thickness.

53. The method of manufacturing the semiconductor device as defined in claim 49, wherein, a thickness of the single-crystal silicon substrate including the dense position is about not more than 100μm.

54. The method of manufacturing the semiconductor device as defined in claim 50, wherein, a thickness of the single-crystal silicon substrate including the dense position is about not more than 100μm.

55. The method of manufacturing the semiconductor device as defined in claim 44, wherein, after the non-single-crystal silicon thin film is formed on the insulating substrate, at least a surface area from which the non-single-crystal silicon is removed and to which a single-crystal silicon is to be bonded is planarized in advance by performing a GCIB (Gas Cluster Ion Beam) using halide in approximately 3keV.

56. A method of manufacturing a semiconductor device, comprising the step of:

(a) bonding an insulating film formed on an insulating substrate with a covering film with which a single-crystal silicon substrate is covered,

the method further comprising the step of:

(b) before the step (a), regulating a tangent of a maximum slope of micro-roughness on a surface of the insulating film to a surface plane of the insulating substrate, measured in a 1-5μm square, is not more than 0.06, the micro-roughness being not more than 5nm in height.